Claims:

1. A standard cell comprising a power supply terminal of a diffused layer, an input terminal of a first level metal and an output terminal of said first level metal.

2. A standard cell claimed in Claim 1, further comprising a function circuit including at least one P-channel transistor and at least one N-channel transistor; a first power supply terminal for supplying a first power supply voltage to said at least one P-channel transistor, a second power supply terminal for supplying a second power supply voltage to said at least one N-channel transistor, and an input terminal and an output terminal for said function circuit, wherein said first power supply terminal is provided at a P-type diffused layer of said at least one P-channel transistor supplied with said first power supply voltage, and said second power supply terminal is provided at an N-type diffused layer of said at least one N-channel transistor supplied with said second power supply voltage, and wherein said input terminal of said first level metal and said output terminal of said first level metal constitute said input terminal and said output terminal for said function circuit, respectively.

3. A standard cell array including a plurality of standard cells formed on a semiconductor substrate and located in the form of an array, each of said standard cells comprising a power supply terminal of a diffused layer, an input terminal of a first level metal and an output terminal of said first level metal, wherein said plurality of standard cells are located in such a manner that respective well boundary lines within said standard cells are aligned on one straight line, and a substrate contact cell for

connecting a first power supply voltage and a second power supply voltage to said semiconductor substrate and a well formed in said semiconductor substrate, respectively, is inserted into said standard cell array at predetermined intervals, at least one for a predetermined number of standard cells.

4. A standard cell placement and routing processing system comprising a library file which stores information of various standard cells each of which comprises a power supply terminal of a diffused layer, an input terminal of a first level metal and an output terminal of said first level metal, a circuit connection information file which stores circuit connection information of an LSI to be developed, a constraint information file which stores constraint information concerning the placement and the routing, a parameter file which stores parameter information including a power supply voltage and an operating frequency of said LSI to be developed and a sheet resistance of said diffused layer, a placement and routing system for executing the placement and the routing of standard cells selected in accordance with the circuit connection information from said circuit connection information file, by utilizing information from said library file, said constraint information file and said parameter file, and an input/output and display apparatus for displaying a history and a result of the placement and the routing and for externally inputting a control command to control said placement and routing system.

5. A standard cell placement and routing method for executing a placement and routing of standard cells by using a standard cell placement

and routing processing system which comprises a library file which stores information of various standard cells each of which comprises a power supply terminal of a diffused layer, an input terminal of a first level metal and an output terminal of said first level metal, a circuit connection information file which stores circuit connection information of an LSI to be developed, a constraint information file which stores constraint information concerning the placement and the routing, a parameter file which stores parameter information including a power supply voltage and an operating frequency of said LSI to be developed and a sheet resistance of said diffused layer, a placement and routing system for executing the placement and the routing of standard cells selected in accordance with the circuit connection information from said circuit connection information file, by utilizing information from said library file, said constraint information file and said parameter file, and an input/output and display apparatus for displaying a history and a result of the placement and the routing and for externally inputting a control command to control said placement and routing system,

the method comprising:

a first step of reading out said circuit connection information from said circuit connection information file;

a second step of reading out from said cell library file, standard cells corresponding to the read-out circuit connection information, and locating the read-out standard cells into a plurality of standard cell arrays, each of said plurality of standard cell arrays including at least one substrate contact cell inserted for every a predetermined number of standards cells, and said standard cells included in each of said plurality of standard cell arrays being arranged in such a manner that respective well

boundary lines within the standard cells in each standard cell array are aligned on one straight line in a plan view;

a third step of routing signal lines between the standard cells included in said standard cell array, in accordance with said circuit connection information;

a fourth step of extracting a contour of a wiring area of said signal lines within said standard cell array, and placing a power supply line at the outside of said wiring area;

a fifth step of forming a contact hole at an overlapping portion between said power supply line and said power supply terminal of said diffused layer within said standard cell in said standard cell array, or alternatively, extending a power supply line of said diffused layer from said power supply terminal to said power supply line when said power supply terminal does not overlap said power supply line, and then, forming a contact hole at an overlapping portion between said power supply line and said power supply line of said diffused layer;

a sixth step of discriminating whether or not the resistance of said power supply line of said diffused layer is not greater than a predetermined resistance value stored in said constraint information file;

a seventh step of re-routing said signal lines between said standard cells when it is discriminated in said sixth step that the resistance of said power supply line of said diffused layer is greater than said predetermined resistance value, and then, returning to said fourth step; and

an eighth step of routing a not-connected interconnection in said standard cell array and signal lines between said standard cell arrays when it is discriminated in said sixth step that the resistance of said power

supply line of said diffused layer is not greater than said predetermined resistance value.

6. A method claimed in Claim 5 wherein said second step includes:

a first sub-step of reading out from said cell library file, said standard cells corresponding to the read-out circuit connection information, and locating said read-out standard cells into a plurality of standard cell arrays in such a manner that respective well boundary lines within the standard cells in each standard cell array are aligned on one straight line in a plan view;

a second sub-step of inserting said at least one substrate contact cell for every a predetermined number of standards cells in each standard cell array, to complete said plurality of standard cell arrays;

a third sub-step of calculating a power supply line width on the basis of information including the number of the standard cells and the kinds of the standard cells included said standard cell array, said power supply voltage, and said operating frequency;

a fourth sub-step of calculating the width of a routing channel required from said power supply line width, the number of signal lines, and signal paths; and

a fifth sub-step of discriminating whether or not the routing is possible, with reference to a chip size stored in said constraint information file, and returning to said first sub-step when the routing is not possible, and on the other hand, completing said second step when the routing is possible.

7. A method claimed in Claim 5 wherein said fifth step includes:

a first sub-step of extracting said power supply terminals of said standard cells included in said standard cell array;

a second sub-step of discriminating whether or not the extracted power supply terminal overlaps said power supply line;

a third sub-step of extending said power supply line of said diffused layer from said extracted power supply terminal to said power supply line when said extracted power supply terminal does not overlap said power supply line, so that said power supply line of said diffused layer overlaps said power supply line; and

a fourth sub-step of forming a contact hole at an overlapping portion between said extracted power supply terminal and said power supply line when it is discriminated in said second sub-step that said extracted power supply terminal overlaps said power supply line, or alternatively at an overlapping portion between said power supply line and said power supply line of said diffused layer when it is discriminated in said second sub-step that said extracted power supply terminal does not overlap said power supply line.

8. A method claimed in Claim 5 wherein said seventh step includes:

a first sub-step of detecting a signal line which becomes a hindrance in reducing the resistance of said power supply line formed of said diffused layer to not greater than said predetermined resistance value;

a second sub-step of removing said signal line which becomes said hindrance, and providing a through-hole for connecting between said first level metal and a second level metal at an end position to which the removed signal line was connected; and

a third sub-step of discriminating whether or not the resistance of said power supply line formed of said diffused layer shortened as the result of the removal of said signal line is not greater than said predetermined resistance value, and returning to said first sub-step when the resistance is greater than said predetermined resistance value, or alternatively completing said seventh step when the resistance is not greater than said predetermined resistance value.

9. A standard cell placement and routing method for executing a placement and routing of standard cells by using a standard cell placement and routing processing system which comprises a library file which stores information of various standard cells each of which comprises a power supply terminal of a diffused layer, an input terminal of a first level metal and an output terminal of said first level metal, a circuit connection information file which stores circuit connection information of an LSI to be developed, a constraint information file which stores constraint information concerning the placement and the routing, a parameter file which stores parameter information including a power supply voltage and an operating frequency of said LSI to be developed and a sheet resistance of said diffused layer, a placement and routing system for executing the placement and the routing of standard cells selected in accordance with the circuit connection information from said circuit connection information file, by utilizing information from said library file, said constraint information file and said parameter file, and an input/output and display apparatus for displaying a history and a result of the placement and the routing and for externally inputting a control command to control said placement and routing system,

the method comprising:

a first step of reading out said circuit connection information from said circuit connection information file;

a second step of reading out from said cell library file, standard cells corresponding to the read-out circuit connection information, and provisionally locating the read-out standard cells into a plurality of provisional standard cell arrays;

a third step of dividing said provisional standard cell array into a plurality of cell groups each including not greater than a predetermined number of standard cells which are located adjacent to one another;

a fourth step of selecting one cell group to be processed, from said plurality of cell groups;

a fifth step of routing signal lines between said standard cells within said one selected cell group, in accordance with the circuit connection information from said circuit connection information file;

a sixth step of extracting a contour of a wiring area of said signal lines within said one selected cell group, to register a power supply line inhibit area in said constraint information file;

a seventh step of placing a power supply line along the outside of said power supply line inhibit area within said one selected cell group;

an eighth step of forming a contact hole at an overlapping portion between said power supply line and said power supply terminal of said diffused layer within said standard cell in said one selected cell group, or alternatively, extending a power supply line of said diffused layer from said power supply terminal to said power supply line when said power supply terminal does not overlap said power supply line, and then,

forming a contact hole at an overlapping portion between said power supply line and said power supply line of said diffused layer;

a ninth step of discriminating whether or not the resistance of said power supply line of said diffused layer is not greater than a predetermined resistance value stored in said constraint information file;

a tenth step of re-routing said signal lines between said standard cells when it is discriminated in said ninth step that the resistance of said power supply line of said diffused layer is greater than said predetermined resistance value, and then, returning to said fifth step;

an eleventh step of discriminating whether or not the processing for all the cell groups has been completed, when it is discriminated in said ninth step that the resistance of said power supply line of said diffused layer is not greater than said predetermined resistance value, and then, returning to said fourth step when the processing for all the cell groups has not yet been completed;

a twelfth step of replacing said provisional standard cell array composed of the provisionally located standard cells, with corresponding cell groups processed above, when it is discriminated in said eleventh step that the processing for all the cell groups has been completed;

a thirteenth step of interconnecting respective power supply lines of said cell groups processed above to form a power supply line for said standard cell array; and

a fourteenth step of routing a not-connected interconnection in said standard cell array and signal lines between said standard cell arrays.